REMARKS

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Applicants assert that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims is respectfully requested.

Status of Claims

Claims 1 through 34 are pending in the application. Claims 3 through 8, and 16 through 34 have been withdrawn from consideration. Claims 1, 2, and 9 through 15 have been rejected.

CLAIM REJECTIONS

35 U.S.C. § 103 Rejections

In the Office Action, the Examiner rejected claims 1,2 and 9 through 15 under 35 U.S.C. § 103(a), as being unpatentable over Eitan et al.,U.S Patent 4,758,869, Mitchell et al.,U.S Patent 5,120,672, Cheung et al., U.S Patent 6,156,149, Wang., U.S Patent 4,992,391 and Kimura et al., U.S Patent 6,195,196.

Applicants respectfully traverse the rejection of claims 1, 2 and 9 through 15 under the above listed combination of separate and unrelated references on the grounds: (1) that the Examiner hasn't shown any motivation to combine any of the cited references, and (2) even if it were proper to combine the cited references, the combination of the references does not teach or suggest all the claimed limitations of independent claim 1.

As the Examiner should well know, the basic rule of law with regards to obviousness type rejections is that in order to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the

art, to modify the reference or to combine reference teachings; second, there must be a reasonable expectation of success; and finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See also MPEP § 2143 - § 2143.03 for decisions pertinent to each of these criteria.

The Examiner appears to have taken the position that there was some motivation to combine four separate reference relating to four separate areas in the general field of semi-conductors in order to obtain all the limitation of claim 1, which claim recites in part:

> "A method of protecting a non-volatile memory device... **(1)** forming a non-volatile memory device comprising a polycide structure formed over a non-conducting charge trapping layer; and **(2)** forming a resistive protective layer over at least a portion of said polycide structure, said **(3)** resistive protective layer adapted to persist on at least a portion of said polycide structure and to absorb electromagnetic wave energy having a wavelength shorter than visible light."

Contrary to what is claimed, the cited references teach:

1. *Eitan et al.* - **Nonvolatile floating gate transistor structure** – A field effect transistor includes a source region, a drain region, and a channel region formed in a semiconductor substrate and a floating gate and a control gate formed over the substrate. An opaque cover (typically aluminum) is formed over but electrically insulated from the transistor to prevent light from striking and affecting the electrical charge on the floating gate. The periphery of the opaque cover ohmically contacts the semiconductor substrate, thereby limiting the amount of light reaching the floating gate, except where the source and drain extend inwardly beyond the periphery of the opaque cover. The control gate extends over

a portion of the substrate surrounding the transistor, and helps hinder light from reaching the floating gate. In addition, semiconductor material formed concurrently with the control gate extends over the source and drain regions, thereby providing additional shading (abstract).

2. *Mitchell et al.* - **Fabricating a single level merged EEPROM cell having an ONO memory stack substantially spaced from the source region** - An electrically, programmable read-only memory cell is formed at a face (10) of a semiconductor layer (12). This cell comprises a doped drain region (36) and a doped source region (38) that are spaced from each other by a gate region (40). An ONO memory stack (28) is formed to extend over a portion of the gate region (40) that adjoins the drain region (36). The memory stack (28) is substantially spaced from the source region (38). A select gate insulator layer (30) is formed over the remainder of the gate region (40), and is preferably of the same thickness as the memory stack (28). A suitable gate conductor (32) is then deposited over insulator layers (26, 30). By being substantially spaced from source region (38), the memory stack (28) of the invention avoids the formation of ONO hole traps (abstract).

3. *Cheung et al.* - **In situ deposition of a dielectric oxide layer and anti-reflective coating** - This invention provides a method and apparatus for depositing a two-layer structure, including an antireflective coating and a dielectric layer, without any intervening process steps, such as a cleaning step. The invention is capable of providing more accurate and easier fabrication of structures by reducing inaccuracies caused by the reflection and refraction of incident radiant energy within a photoresist layer used in the patterning of the dielectric layer. Additionally, the antireflective coating of the present invention may also serve as an etch stop layer during the patterning of a layer formed over the antireflective coating (abstract).

4. *Wang* - **Process for fabricating a control gate for a floating gate FET** - A process of forming a floating gate field-effect transistor having a multi-layer control gate line is disclosed. The multi-layer control gate line includes a first polysilicon layer, a silicide layer provided on the first polysilicon layer, and a second polysilicon layer provided on the silicide layer. The first and second polysilicon layers are formed as undoped polysilicon to improve the adhesion of the polysilicon layers to the silicide layers sandwiched therebetween. After all three layers are formed, the polysilicon layers are doped in an environment including POCl.sub.3. Because the first and second polysilicon layers are formed as undoped layers, all three layers of the control gate line may be formed using a single pump-down.

Although the Eitan reference teaches forming an electromagnetic ration shielding layer on to a "floating gate" device, both the device structure and the protective material used to protect the structure are substantially different in the Eitan reference than what is claimed. More specifically, Eitan teaches protecting a "floating gate" device using an opaque cover, typically aluminum. Conversely, claim 1 recites the limitations of a "polycide structure formed over a non-conducting charge trapping layer" and a "resistive protective layer adapted to persist on at least a portion of said polycide structure and to absorb electromagnetic wave energy having a wavelength shorter than visible light." The main distinctions between what is claimed and what is shown in the Eitan reference are:

No.	Eitan Reference	Claim 1
1.	Floating Gate – Conductive Charge Trapping Layer	Non – Conducting Charge Trapping Layer
2.	Protective Element - opaque cover (typically aluminum)	Protective Element – resistive material
3.	Not Shown	Polycide Structure

The Examiner has asserted that although the above listed elements are absent from the Eitan reference, this defect may be partially cured by combining the Eitan reference with: (1)

the Mitchell reference which teaches an Oxide-Nitride-Oxide (ONO) charge trapping layer in memory cell, (2) the Cheung reference which teaches forming a protective layer to absorb light for antireflective purposes, and (3) the Wang reference discloses a non-volatile memory with a polycide structure and an additional layer over the non-volatile memory.

Applicant asserts that the Examiner used impermissible hindsight to reconstruct the Applicant's invention by using the Applicant's structure as a template and selecting elements from the references to fill the gaps (see In re Gorman, 933 F.2d 982, 18 USPQ2d 1885 (Fed. Cir. 1991). Applicant notes that for the purpose of considering whether a suggested combination may be used to establish implicit teaching, motivation, or suggestion, the references to be combined must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination.

> "[T]he test for establishing an implicit teaching, motivation, or suggestion is what the combination of these two statements of Evans would have suggested to those of ordinary skill in the art, the two statements cannot be viewed in the abstract...Rather, they must be considered in the context of the teaching of the entire reference." *In re Kotzab,* 208 F.3d 1352, 54 USPQ2d 1308 (Fed. Cir. 2000)

Applicant respectfully asserts that an adequate consideration of the prior art cited by the Examiner as a whole, could not have been used to establish sufficient implicit teaching, motivation, or suggestion of the present invention.

More specifically, although the Mitchell reference teaches a non-conducting charge trapping layer (e.g. ONO), there is no suggestion in either Eitan or Mitchell, one of which teaches a "floating gate" device and the other an NROM device, for their teachings to be combined. As is well known in the art, the fabrication and the operation of floating gate and NROM devices are quite different, and transforming one type of device into another is a significant undertaking.

Even if the Examiner had shown sufficient motivation to combine the teachings of Mitchell with those of Eitan, the Examiner admitted that the claimed limitations of a (1) polycide structure and (2) resistive protective layer are absent were still missing. Those

limitations the Examiner found in the Wang and Cheung references, respectively. Once again, however, the Examiner failed to explain why one of ordinary skill in the art would combine the teachings of these references with those of Eitan and Mitchell.

Furthermore, the Examiner mistakenly confused the anti-reflective layer of Cheung, which is specifically intended to "reduce inaccuracies caused by the reflection and refraction of incident radiant energy within a photoresist layer used in the patterning of the dielectric layer" with the resistive proactive layer of claim 1 which is explicitly intended to "protect[ing] a non-volatile memory device."

The Examiner also appears to have been mistaken when citing the Cheung reference, which reference teaches the use of polycide for a floating gate device. As mentioned above, floating gate devices have conducting charge trapping layers. Whereas, Claim 1 specifically states the limitation of a "non-conducting charge trapping layer." Given the difference in fabrication technologies used for floating gate and NROM cells, Applicant asserts it would not have been obvious to combine the teaching of Cheung with the other three cited reference in order to obtain all the limitation of claim 1.

In addition, Applicant respectfully asserts that the teachings of the cited references are not sufficient to render the claims *prima facie* obvious, because the proposed modifications that would be necessary in order to construct a device in accordance with the teachings of the primary reference when combined with the teachings of the THREE secondary references, require, *inter alia*, substantial reconstruction and redesign of the elements shown in the primary reference (see MPEP 2143.01). In *In re Ratti* the court reversed an obviousness type rejection holding that:

> "[the] suggested combination of references would require a substantial reconstruction and redesign of the elements shown in [the primary reference] as well as a change in the basic principle under which the [primary reference] construction was designed to operate." *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)

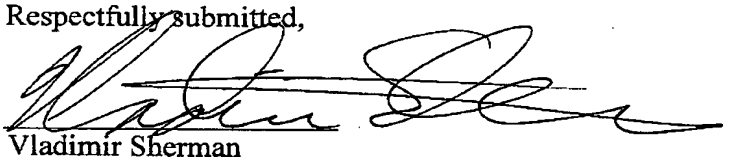
Therefore, Applicant asserts that at least two or more of the four cited references used by the Examiner to support his obviousness rejection may be not be properly combined with the teachings of the others to show all the limitations of claim 1. Even if the combination of all four references was appropriate, the four references combined still fail to teach or suggest all the limitation of claim 1.

Thus, Applicant respectfully requests withdrawal of Examiner's rejections of claim 1. All the pending dependent claims are considered to be allowable by virtue of their dependence on allowable independent claim 1. In view of the foregoing remarks, all pending claims are considered to be allowable. Their favorable reconsideration and allowance is respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Please charge any fees associated with this paper to deposit account No. 50-3400.

Respectfully submitted,



Vladimir Sherman
Attorney for Applicant(s)
Registration No. 43,116

Dated: October 2, 2005

Eitan Law Group, LLP.
C/O Landon IP Inc.
1700 Diagonal Road, Suite 450
Alexandria, VA 22314
Tel: (703) 486-1150
Fax: (703) 892-4510